

Fig. 1A
SIDE VIEW

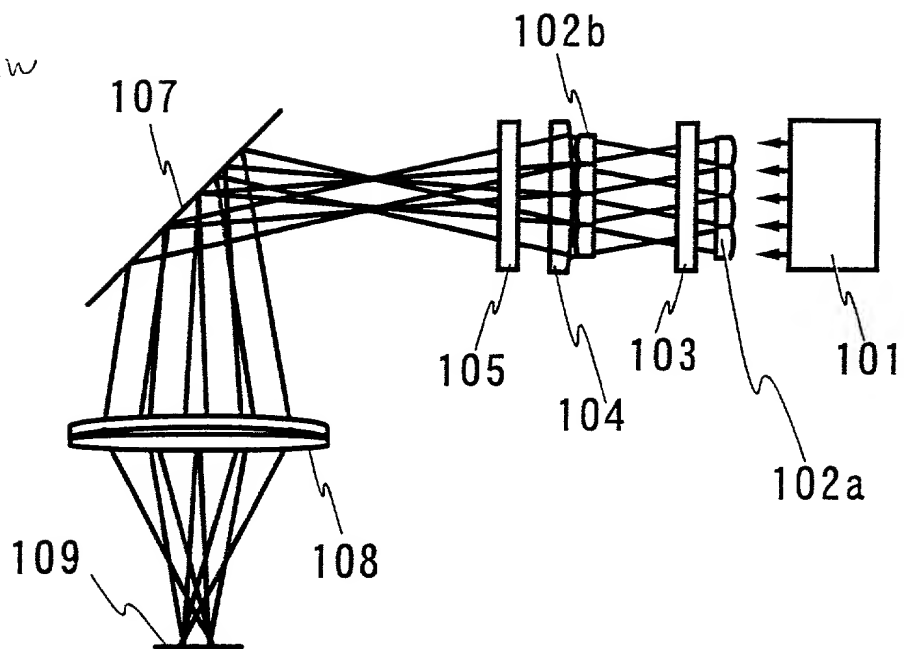
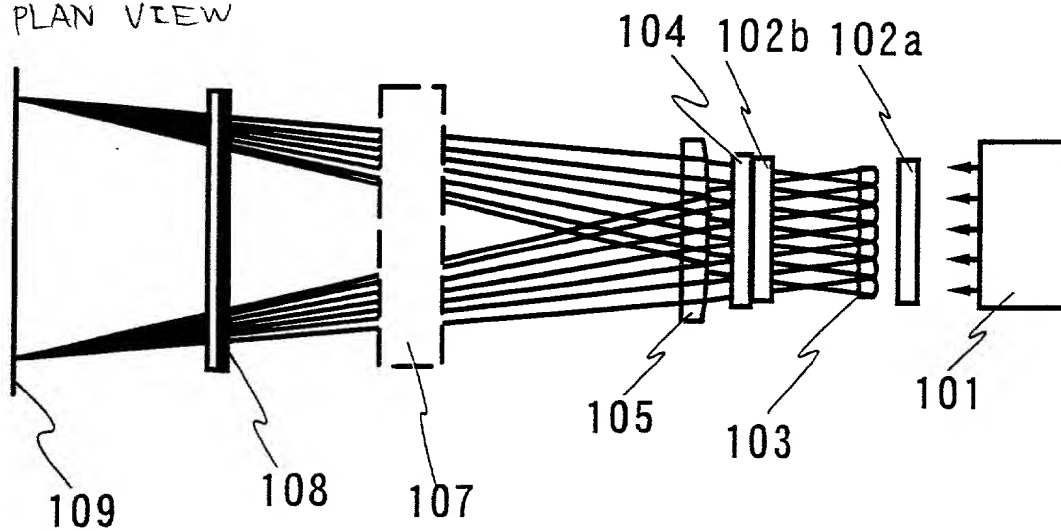


Fig. 1B
PLAN VIEW



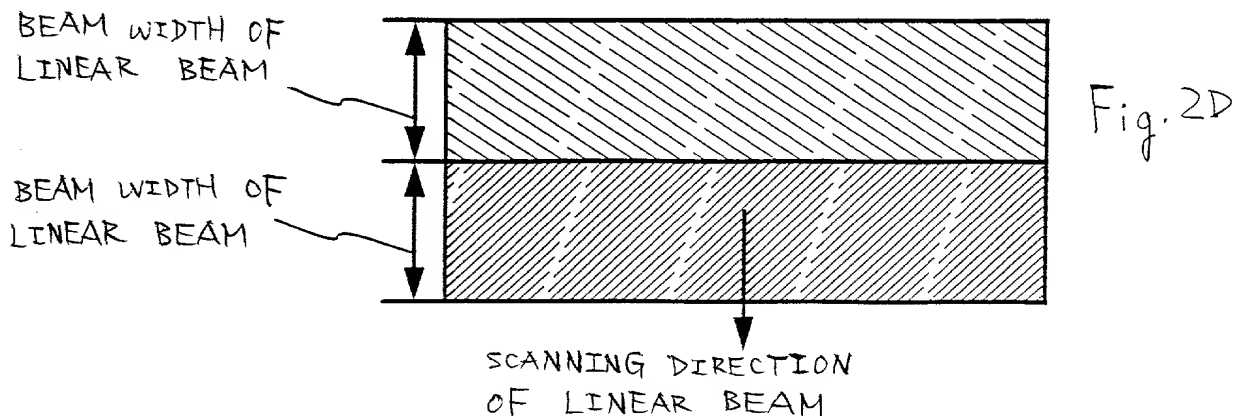
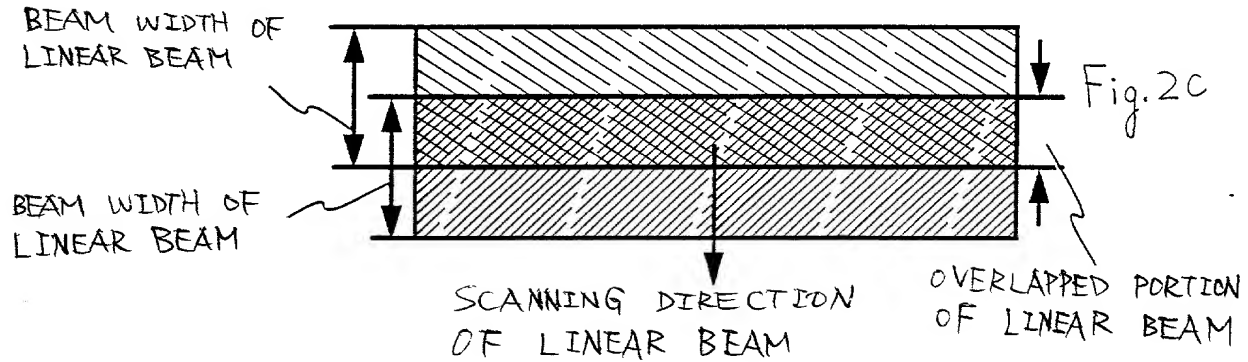
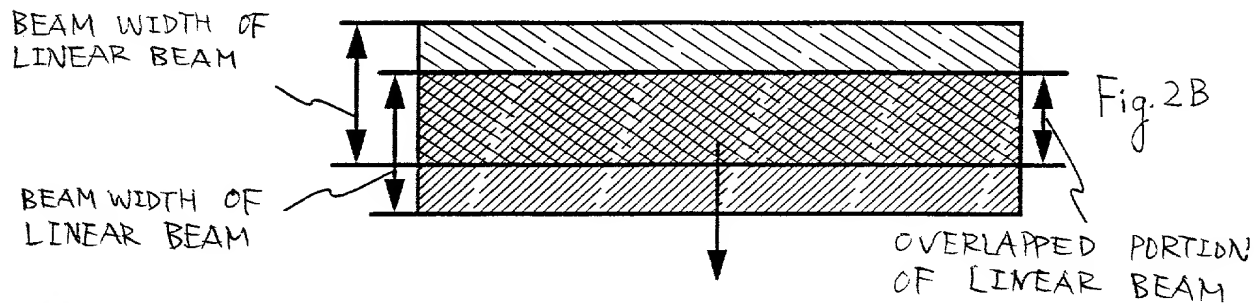
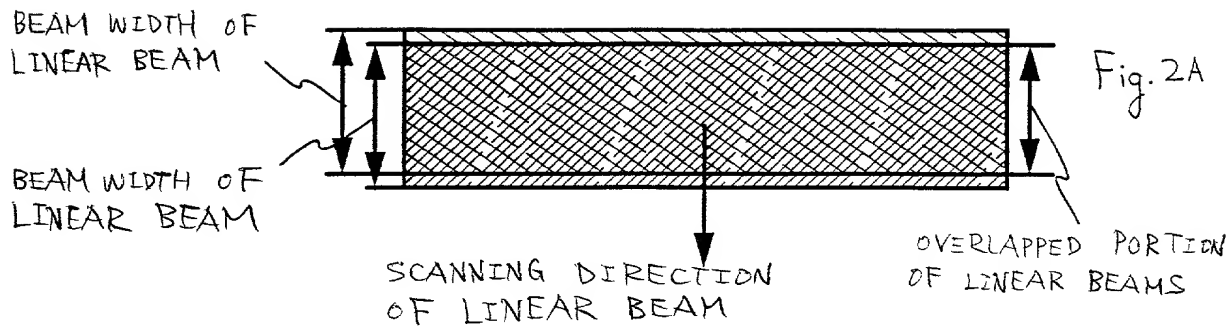


Fig. 3

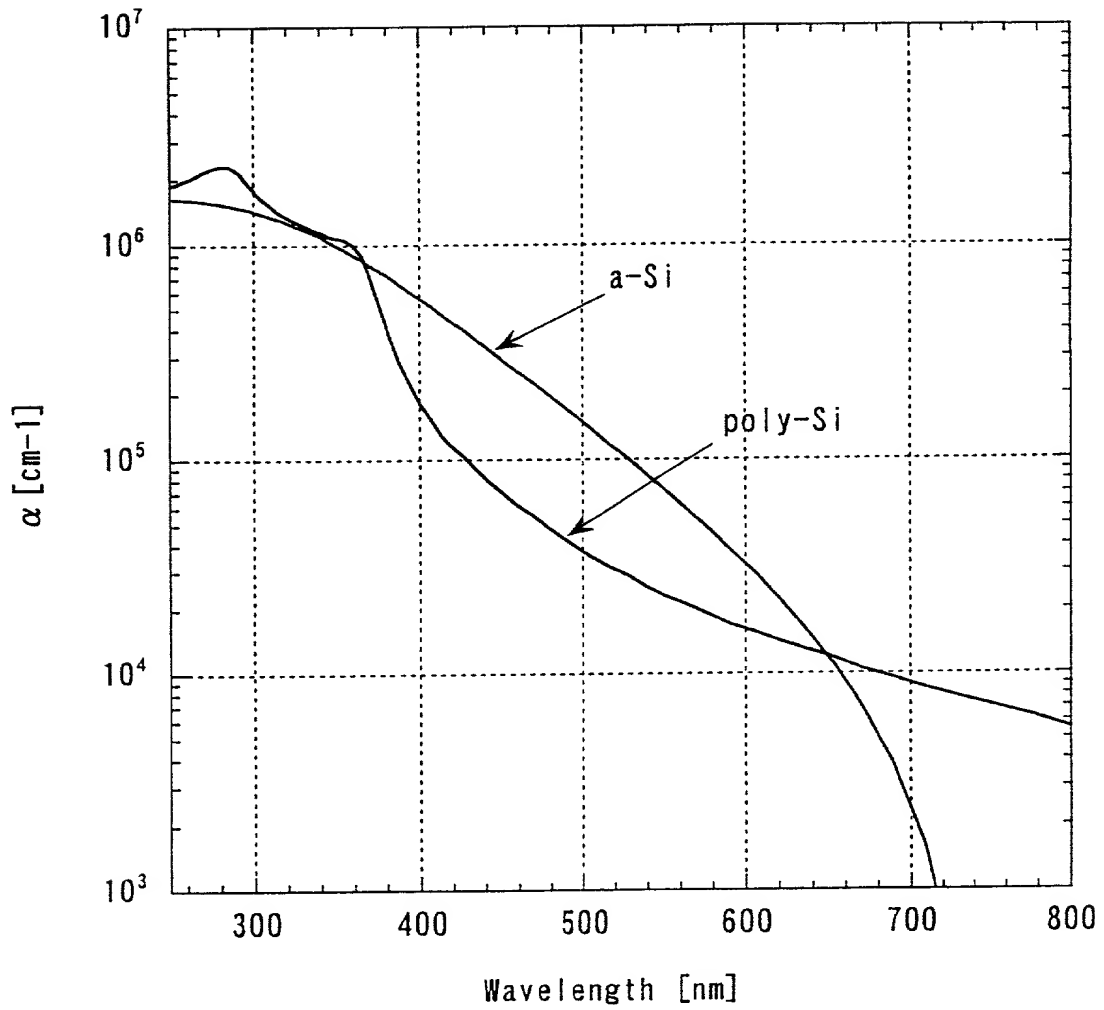


Fig. 4A

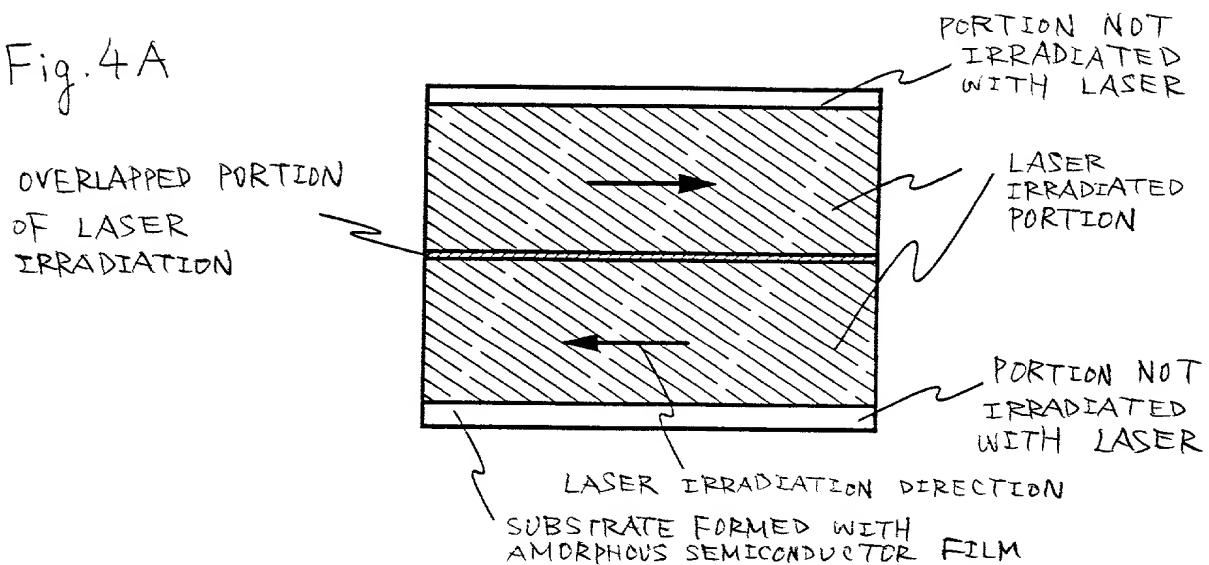


Fig. 4B

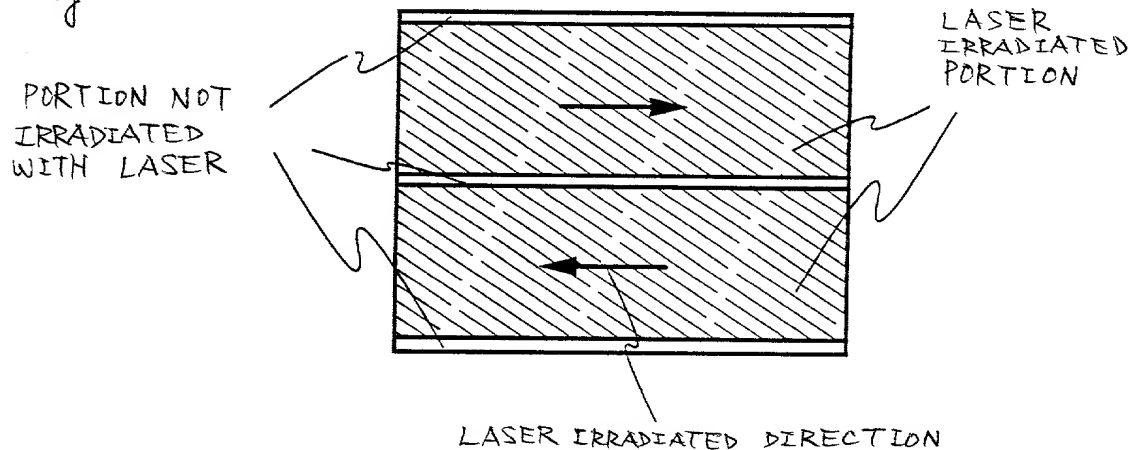


Fig. 4C

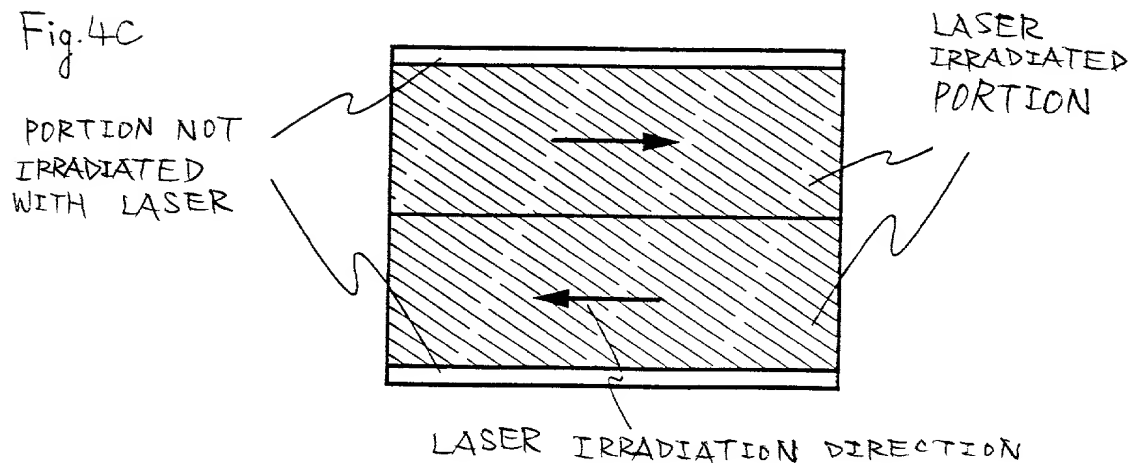


Fig. 5A

SIDE VIEW

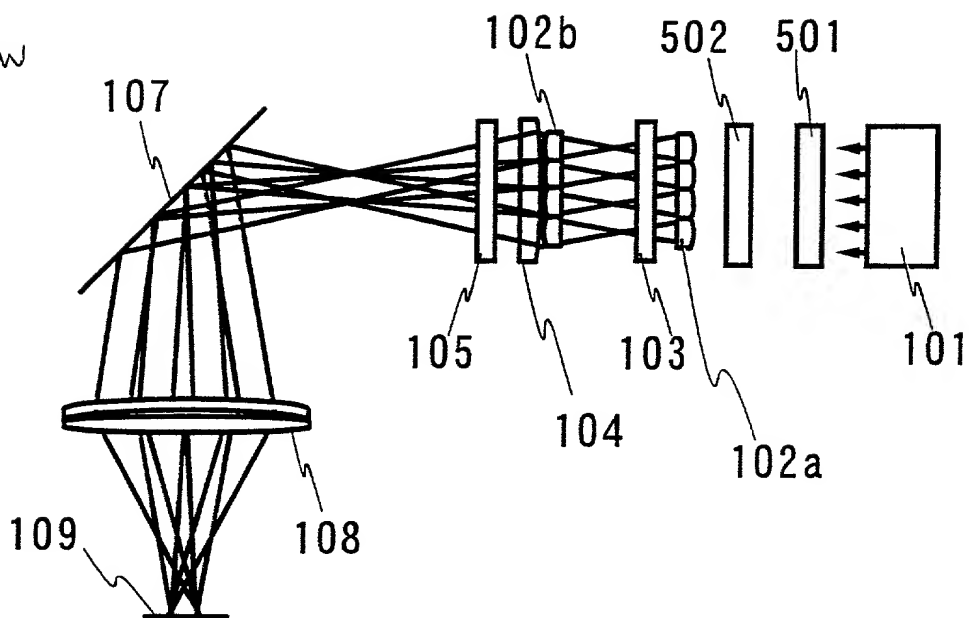
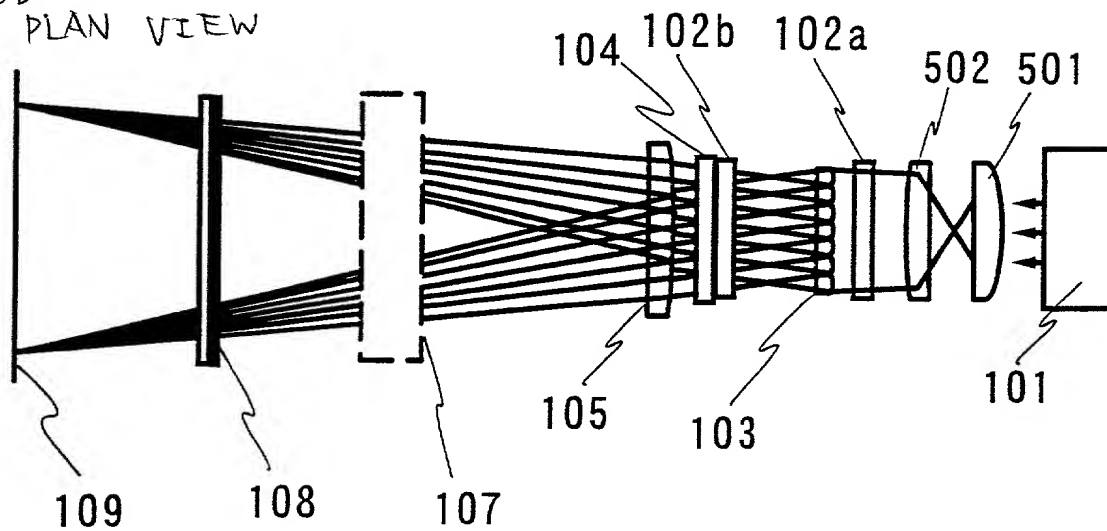


Fig. 5B

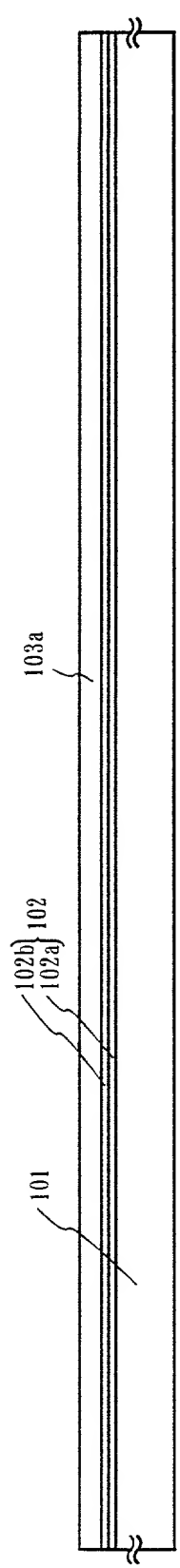
PLAN VIEW



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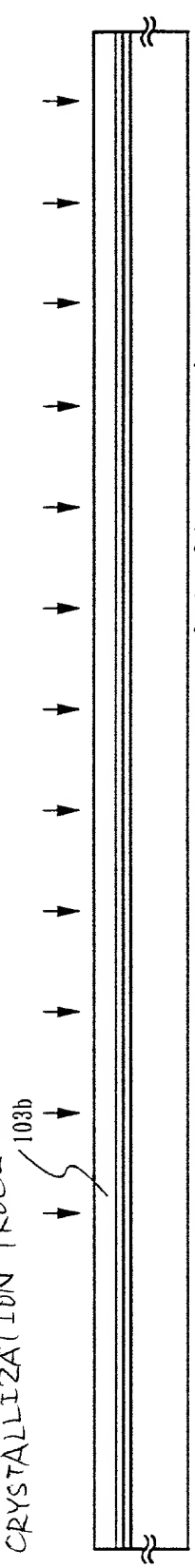
FORMATION OF UNDERLYING FILM AND AMORPHOUS SEMICONDUCTOR FILM

Fig. 6A



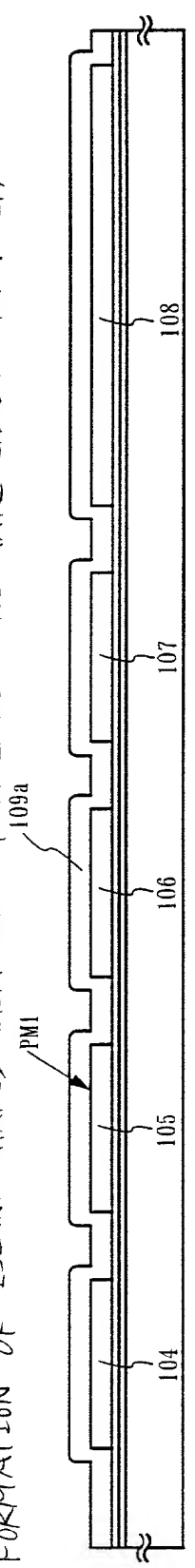
CRYSTALLIZATION PROCESS

Fig. 6B



FORMATION OF ISLAND-SHAPED SEMICONDUCTOR LAYER AND GATE INSULATING FILM

Fig. 6C



FORMATION OF HEAT-RESISTANT CONDUCTIVE LAYER

Fig. 6D

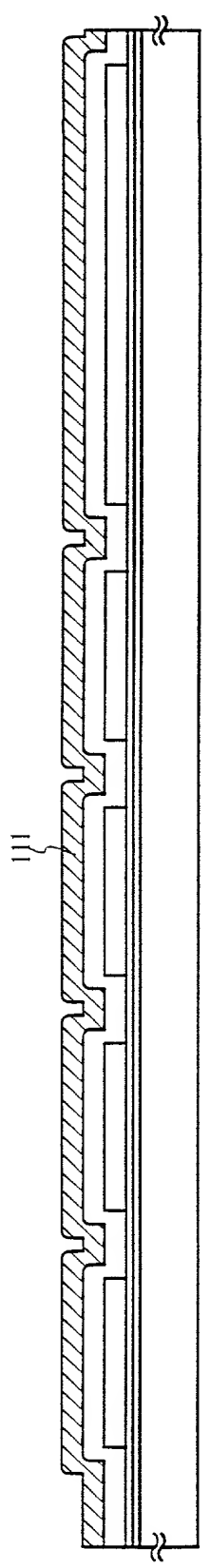
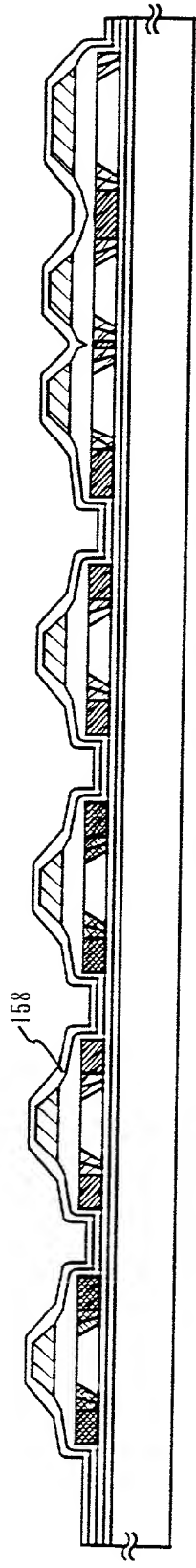


Fig. 8A FORMATION OF FIRST INTERLAYER INSULATING FILM



FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE

Fig. 8B

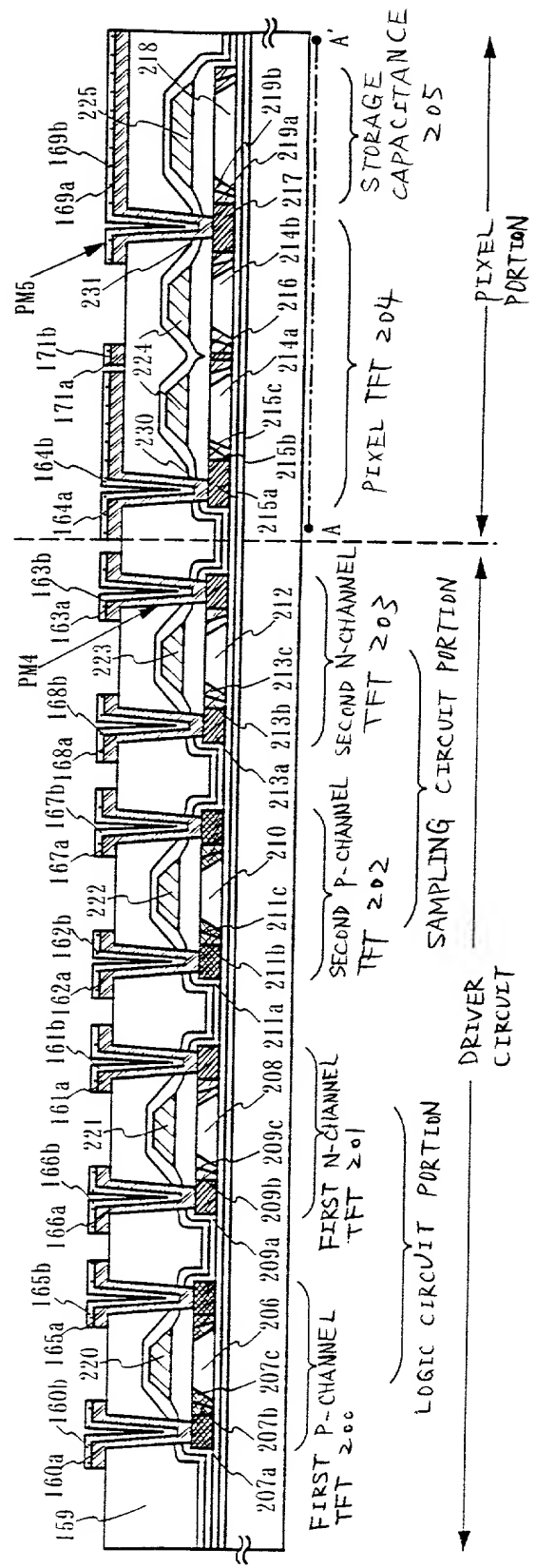
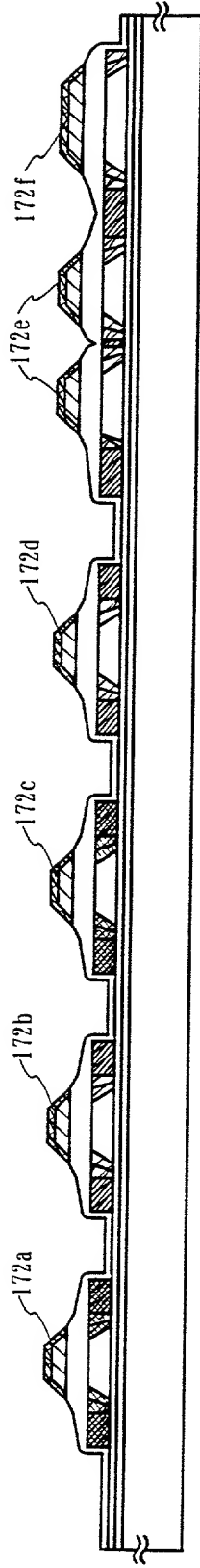
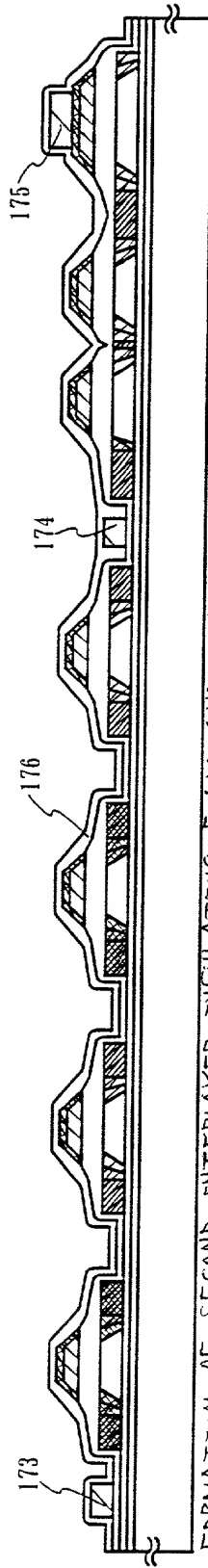


Fig. 9A



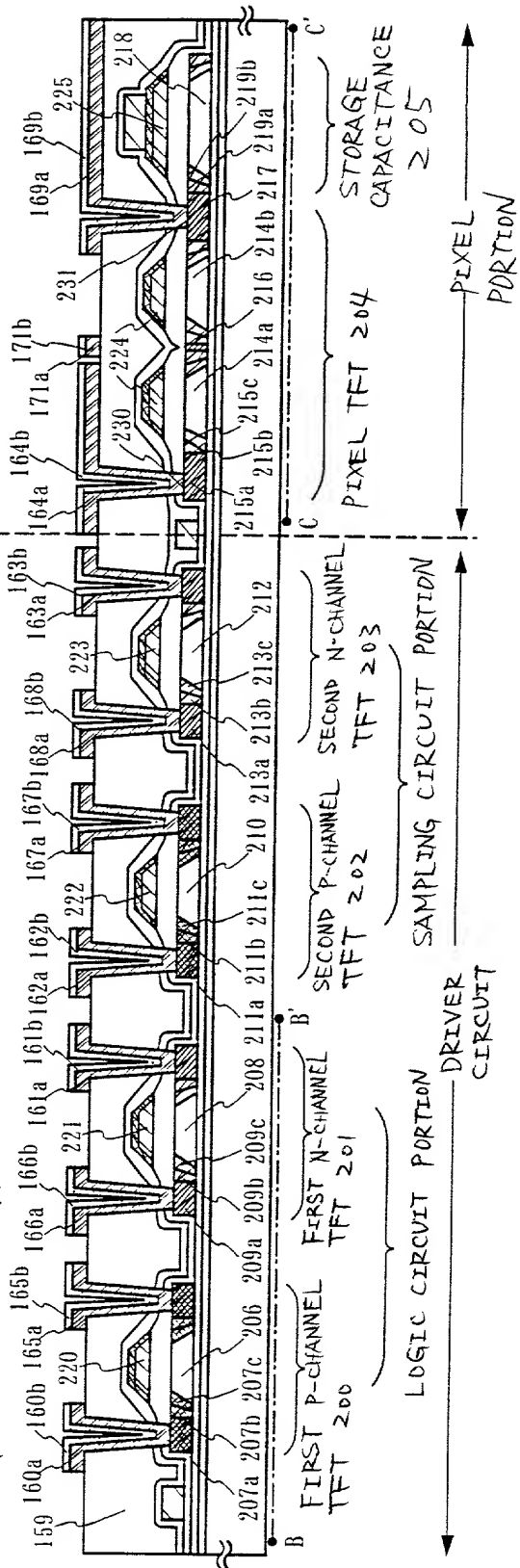
FORMATION OF FIRST INTERLAYER INSULATING FILM

Fig. 9B



FORMATION OF SECOND INTERLAYER INSULATING FILM AND CONTACT HOLE AND WIRING

Fig. 9C



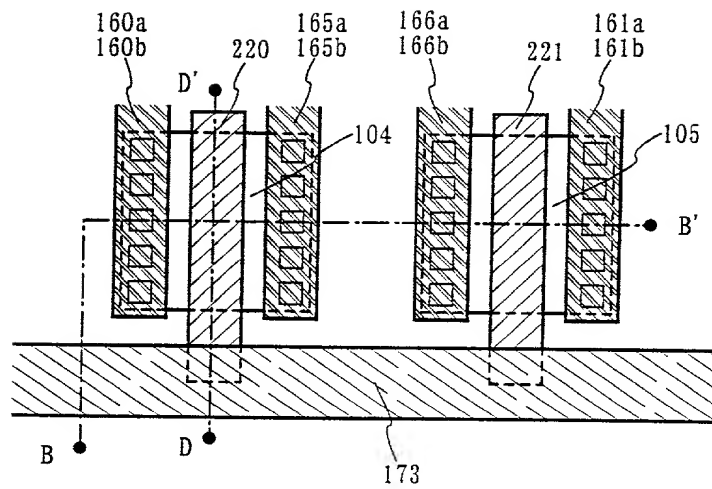


Fig. 10A

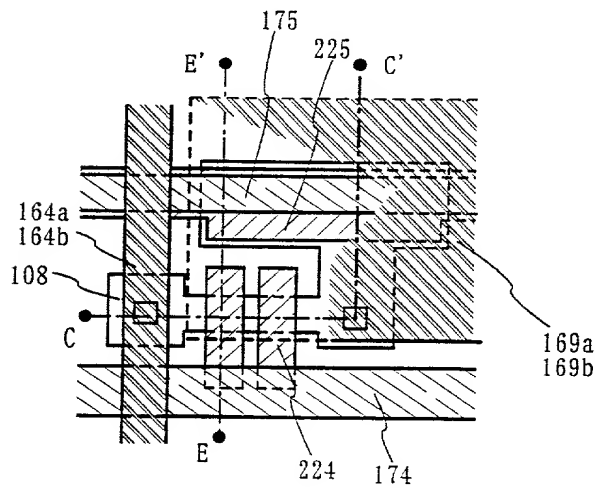


Fig. 10B

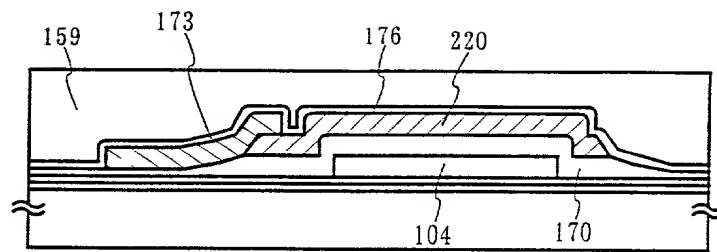


Fig. 11A

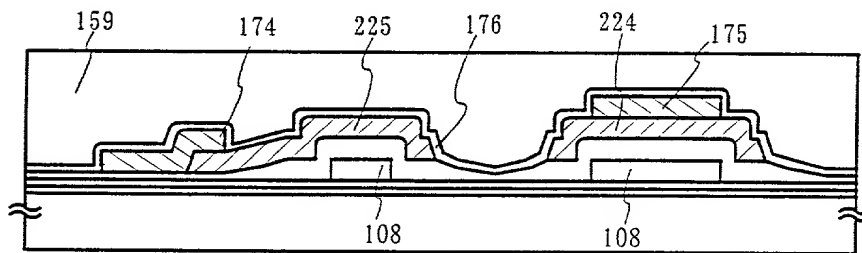
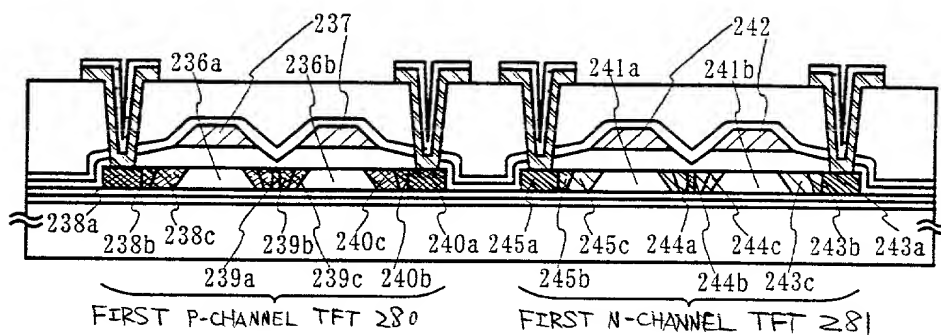
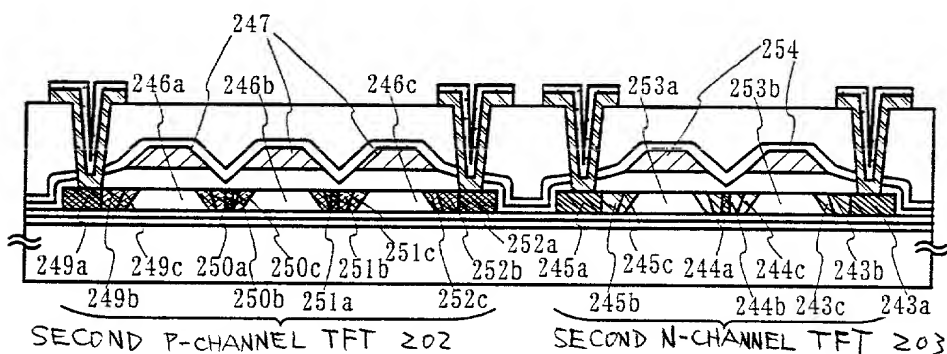


Fig. 11B



LOGIC CIRCUIT PORTION



SAMPLING CIRCUIT PORTION

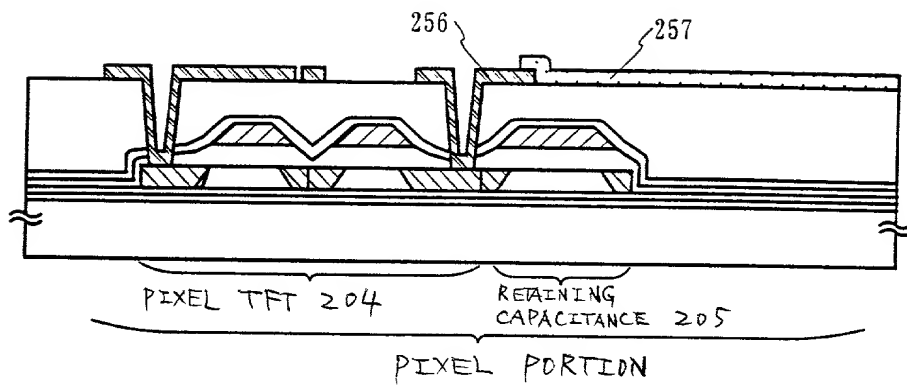


Fig. 13A

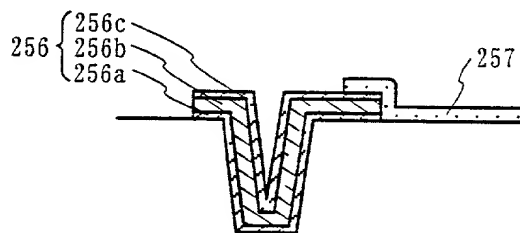


Fig. 13B

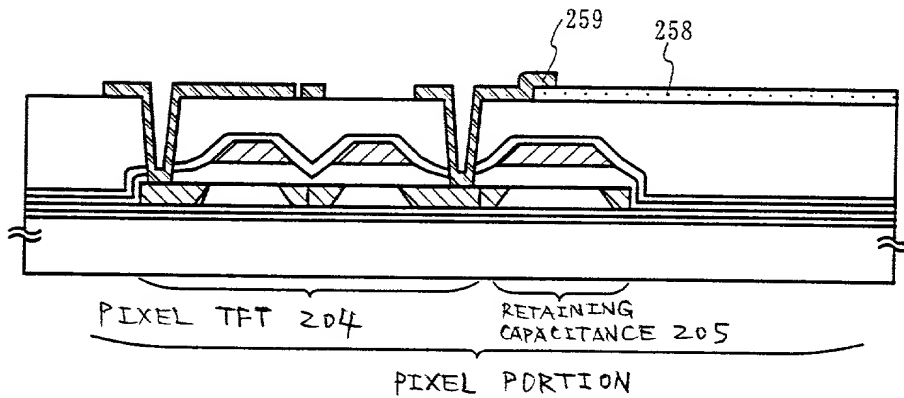


Fig. 13C

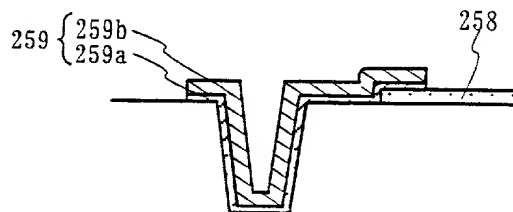


Fig. 13D

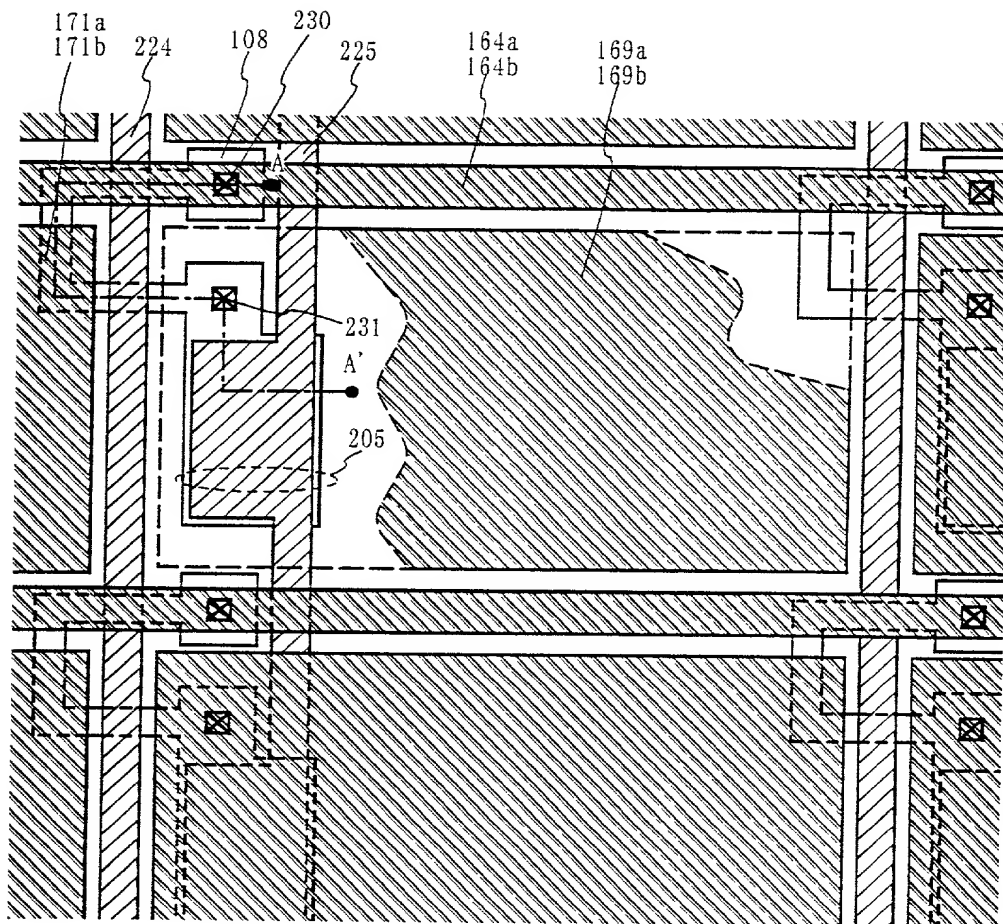
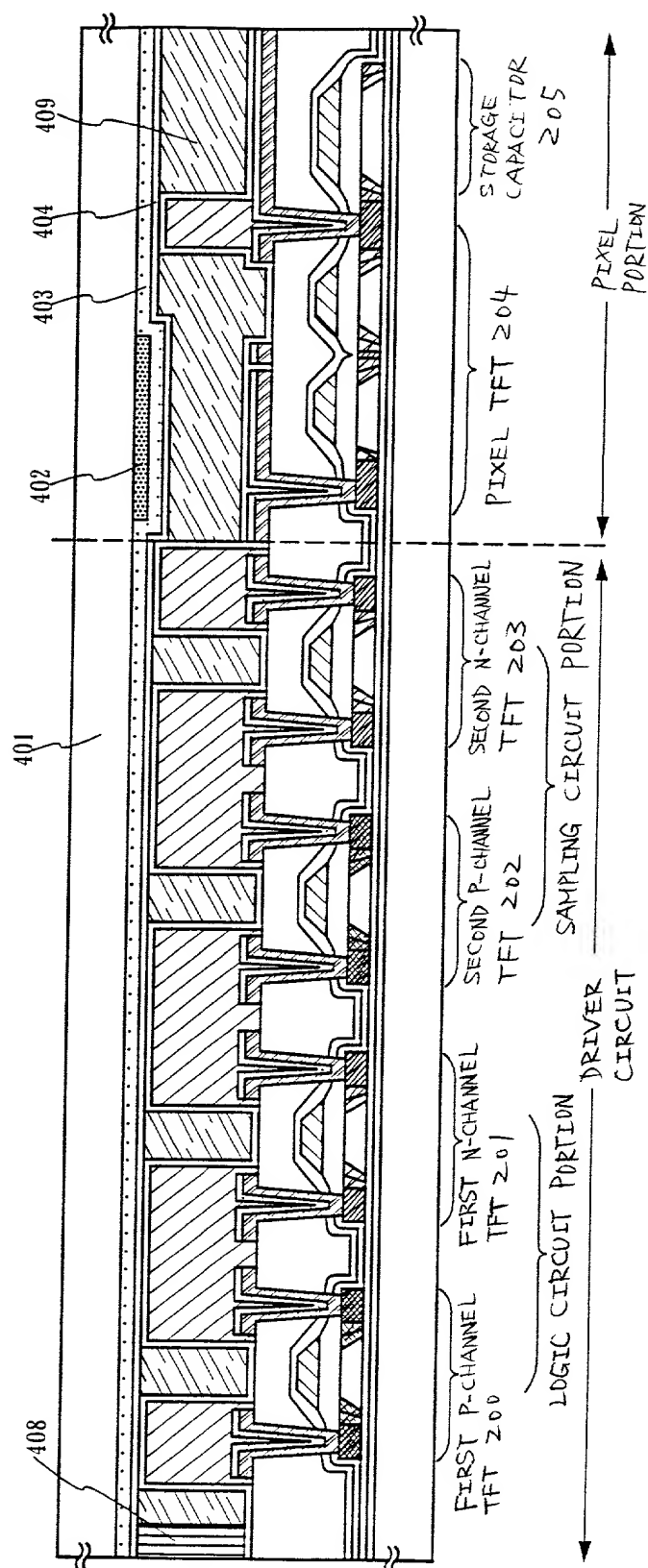
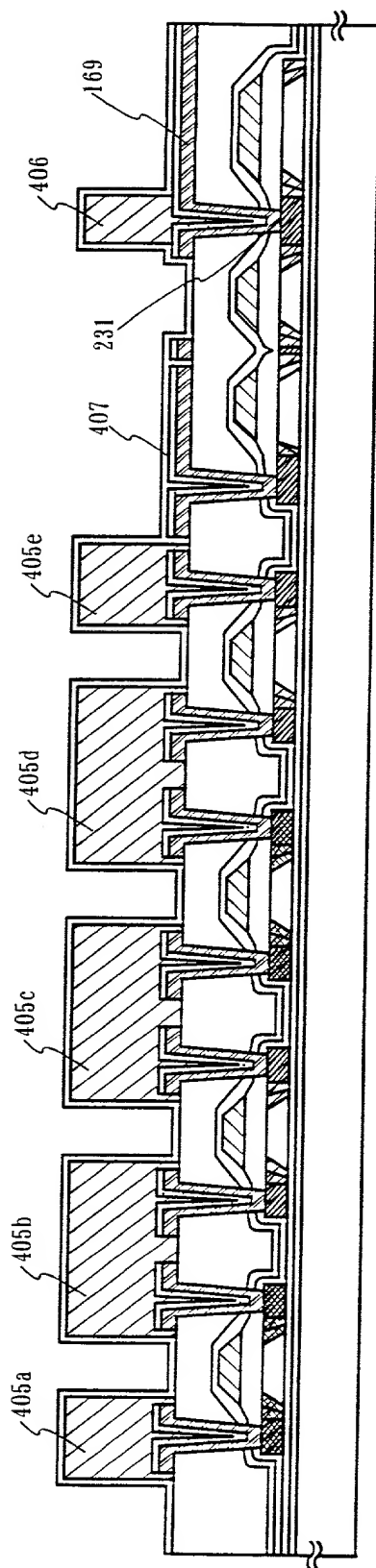


Fig. 14



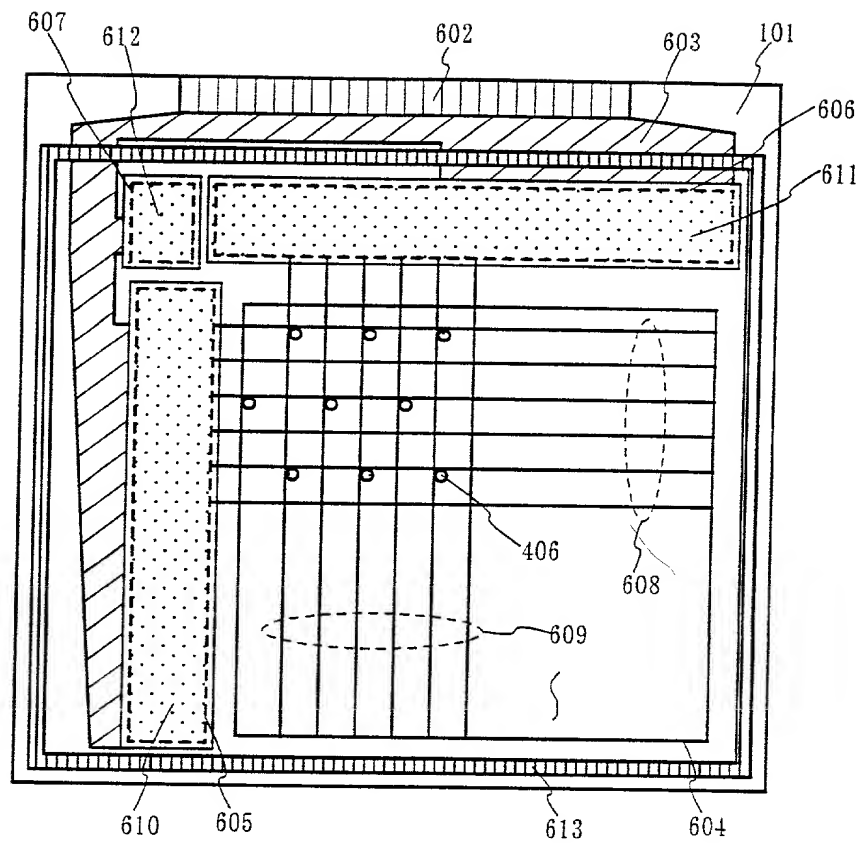
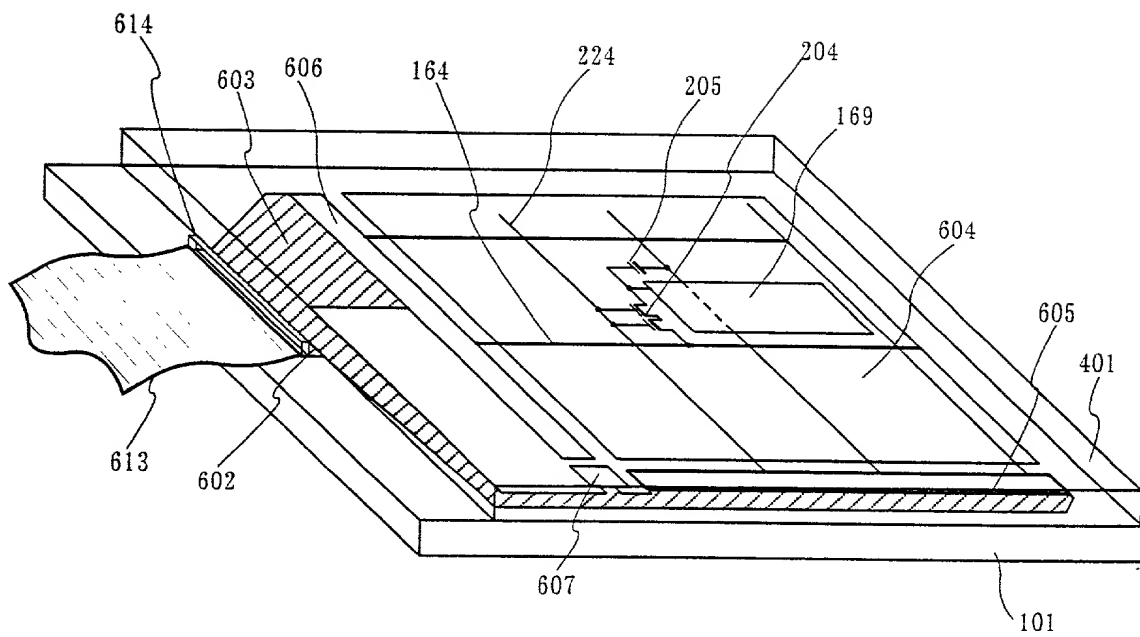


Fig. 16



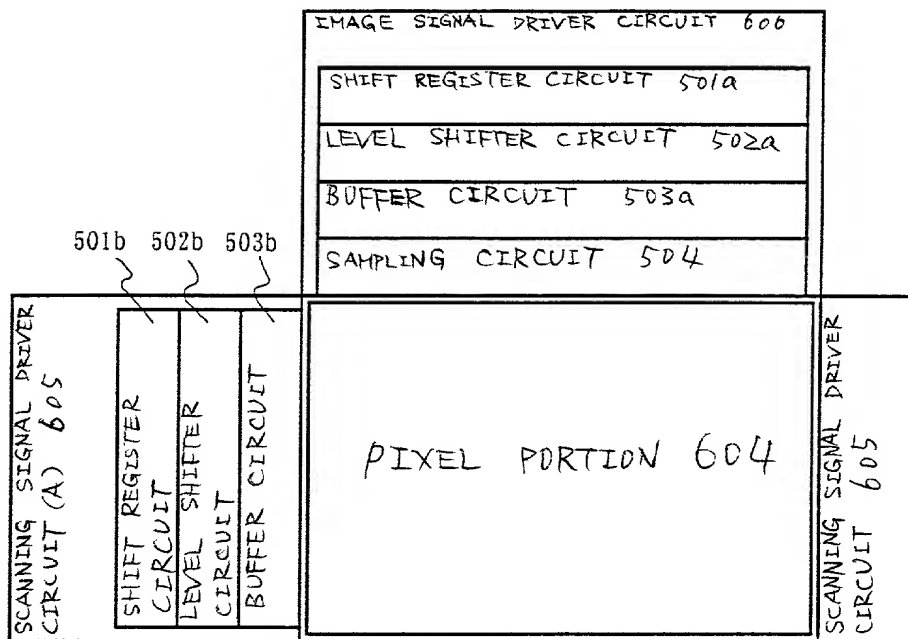


Fig. 18

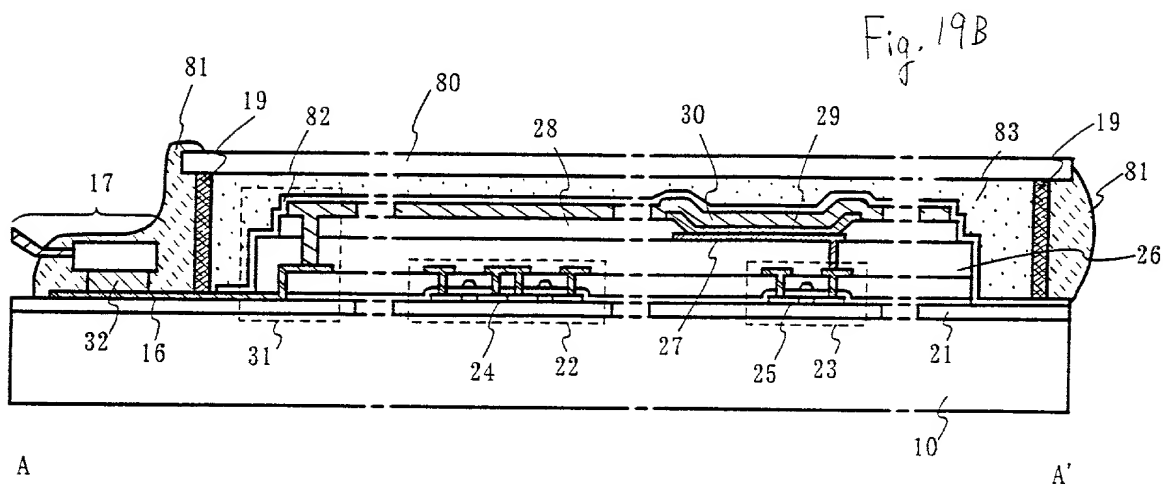
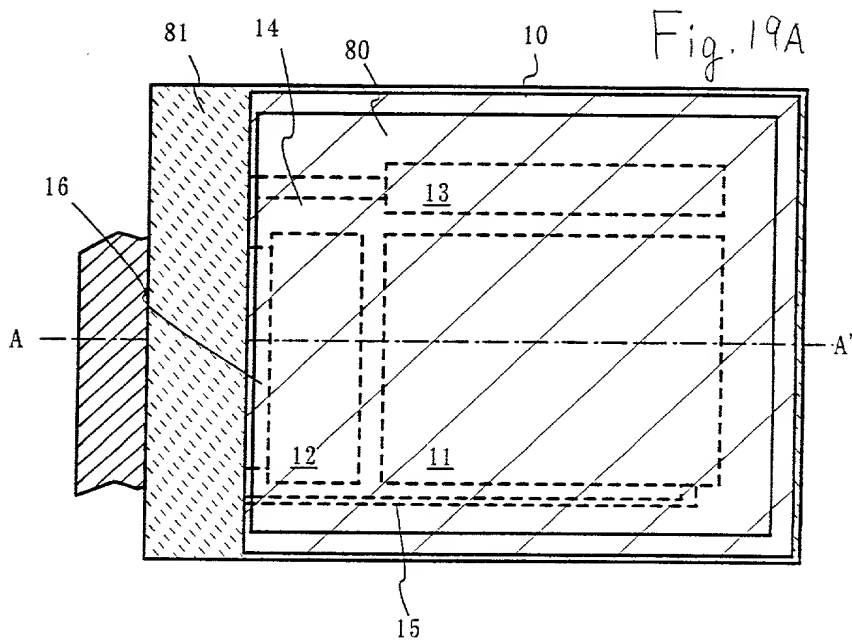


FIG. 20A is a cross-sectional view of a pixel structure in a first embodiment of the present invention. The pixel structure includes a switching TFT 2402, an EL element 2405, and a current controlling TFT 2403. The switching TFT 2402 includes a gate 36, a source 35, and a drain 39a. The EL element 2405 is connected to the drain 39a of the switching TFT 2402 and includes a cathode 44a and an anode 48. The current controlling TFT 2403 includes a gate 42, a source 40, and a drain 44b. The gate 42 of the current controlling TFT 2403 is connected to the gate 36 of the switching TFT 2402. The source 40 of the current controlling TFT 2403 is connected to the source 35 of the switching TFT 2402. The drain 44b of the current controlling TFT 2403 is connected to the anode 48 of the EL element 2405. The pixel structure is formed on a substrate 2401. The gate 36 of the switching TFT 2402 is formed by a layer 37. The gate 42 of the current controlling TFT 2403 is formed by a layer 43. The source 35 of the switching TFT 2402 is formed by a layer 38. The source 40 of the current controlling TFT 2403 is formed by a layer 41. The drain 39a of the switching TFT 2402 is formed by a layer 39b. The cathode 44a of the EL element 2405 is formed by a layer 46. The anode 48 of the EL element 2405 is formed by a layer 47. The current controlling TFT 2403 is formed by a layer 44b. The pixel structure is formed on a substrate 2401.

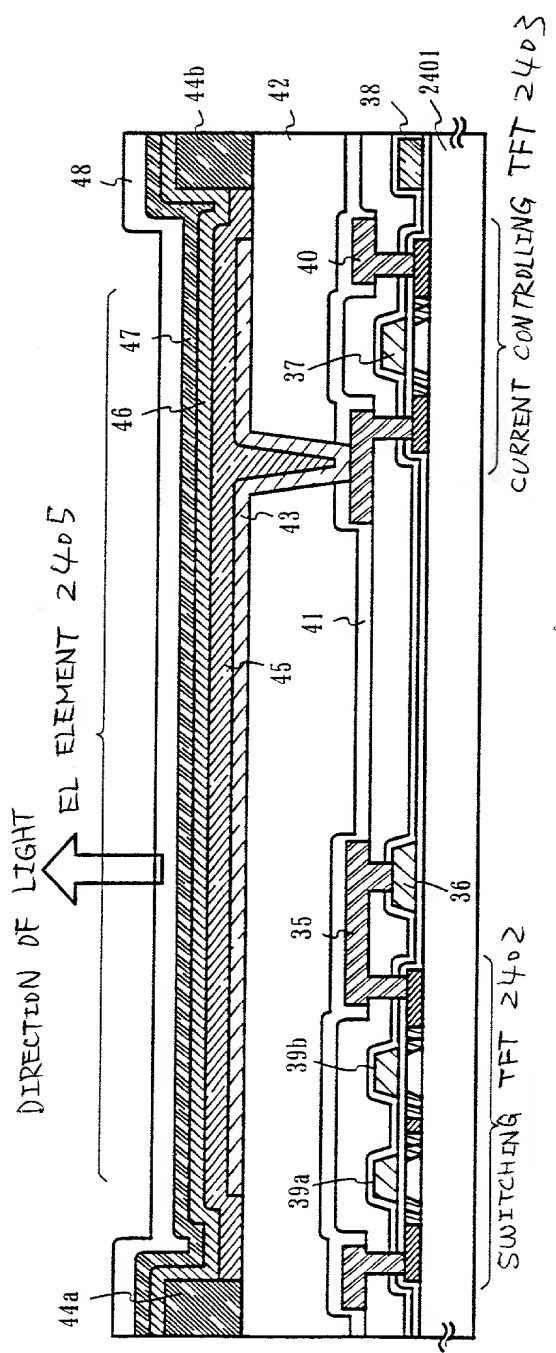


Fig. 20A

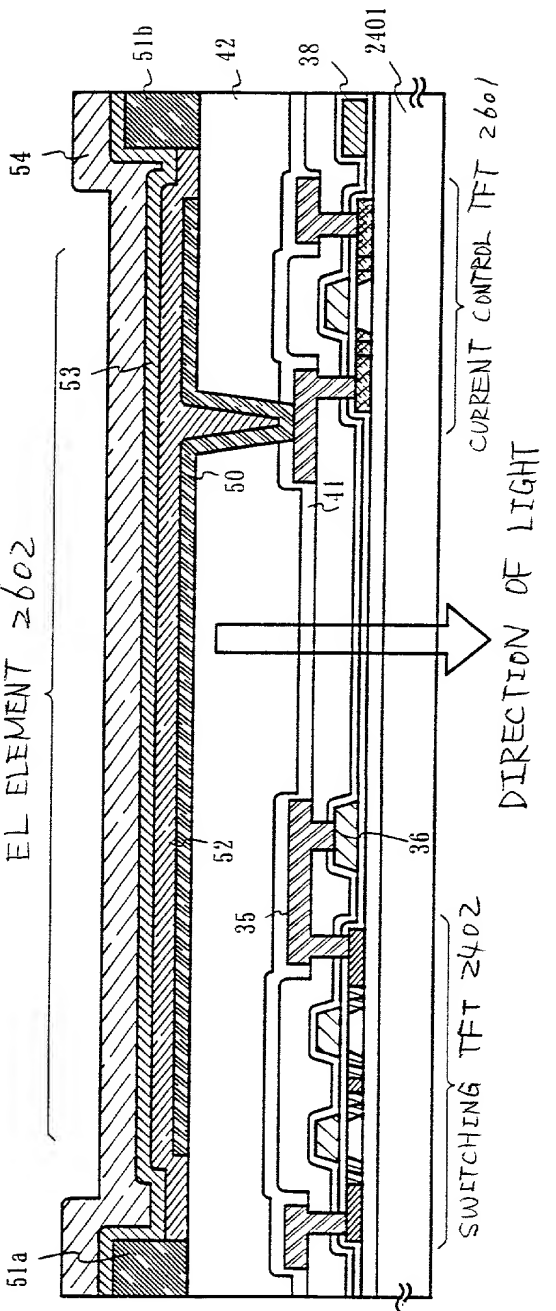
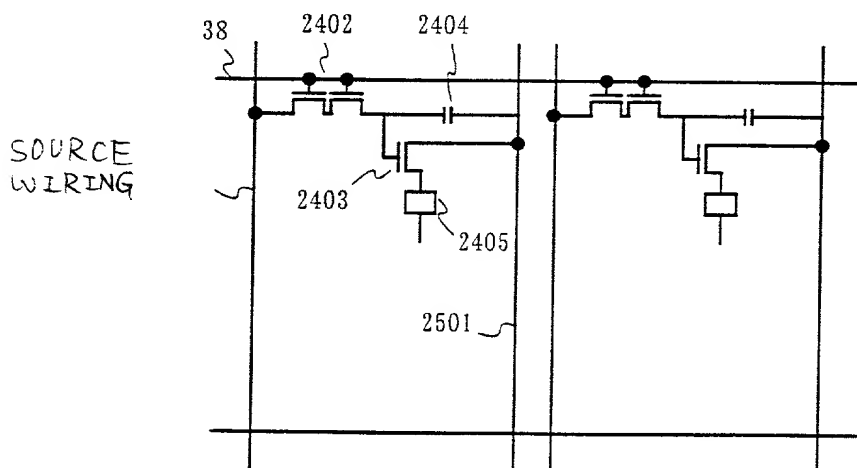
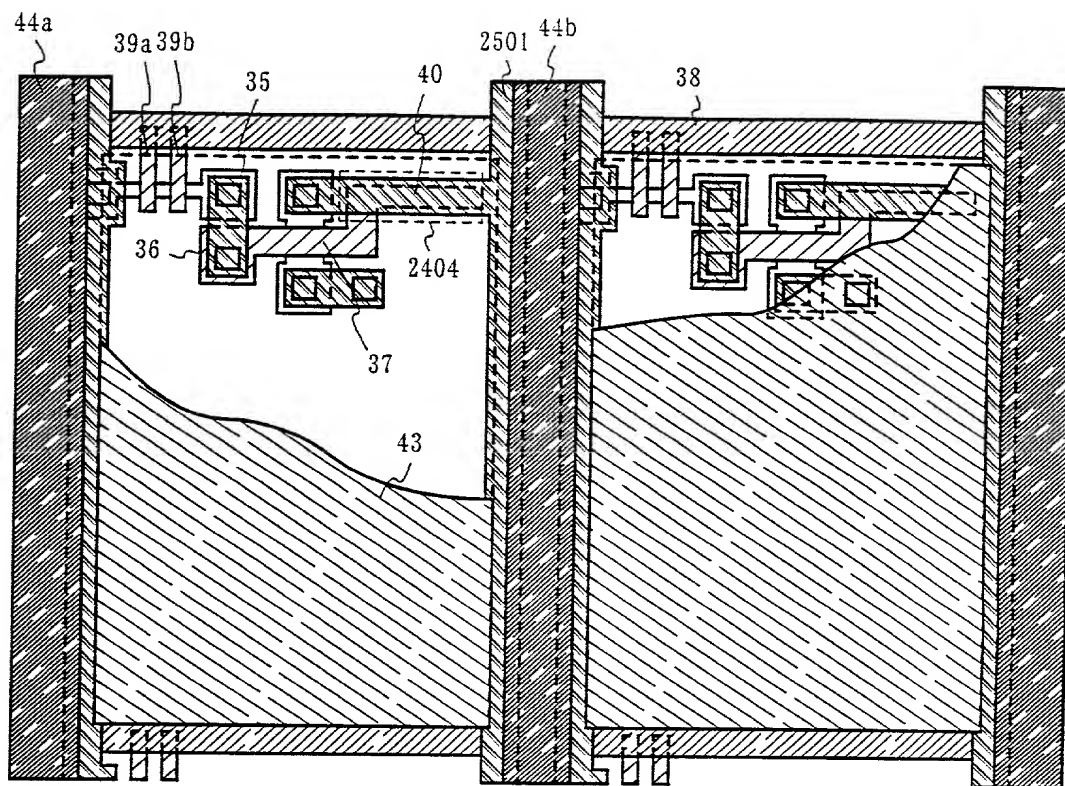


Fig. 20B



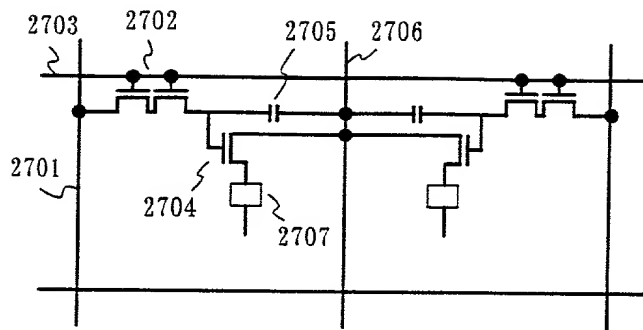


Fig. 22A

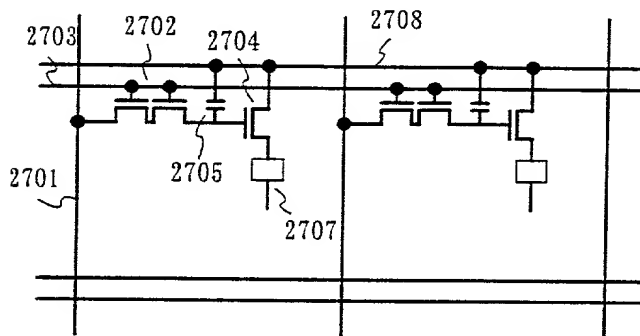


Fig. 22B

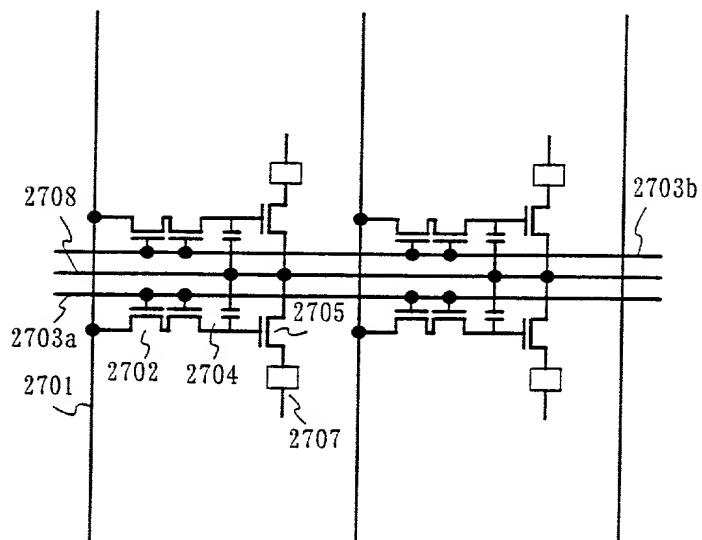


Fig. 22C

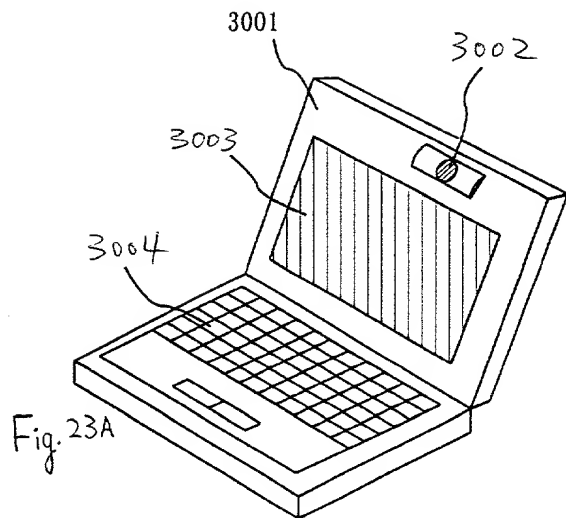


Fig. 23A

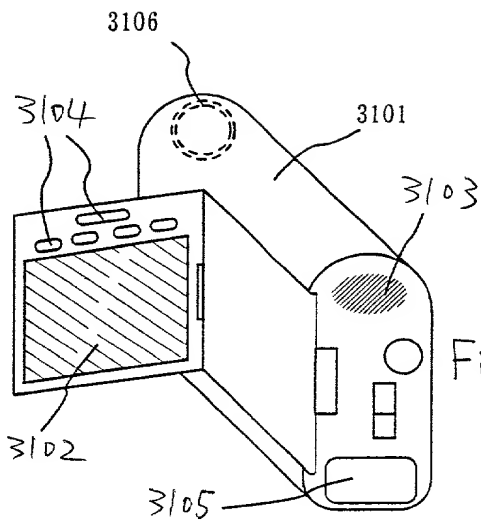


Fig. 23B

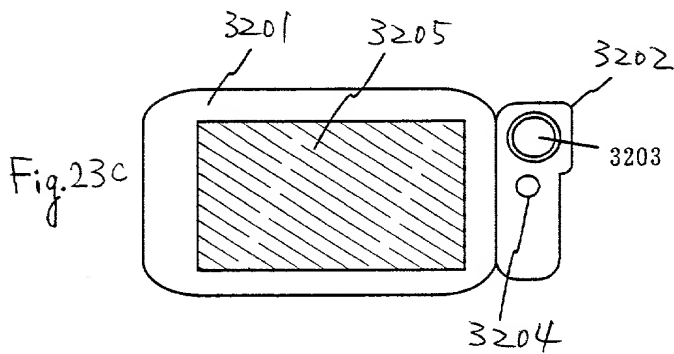


Fig. 23C

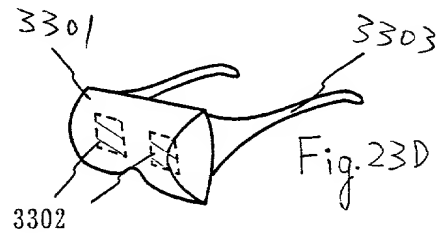


Fig. 23D

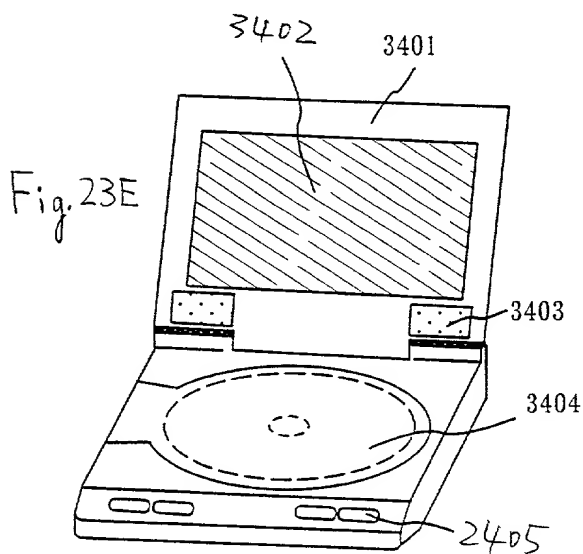


Fig. 23E

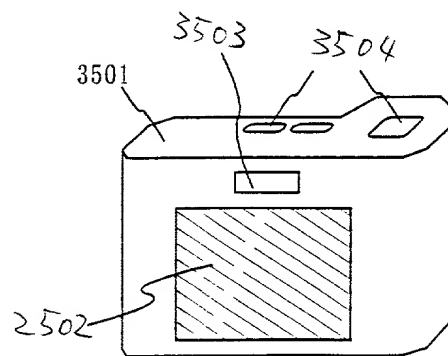


Fig. 23F

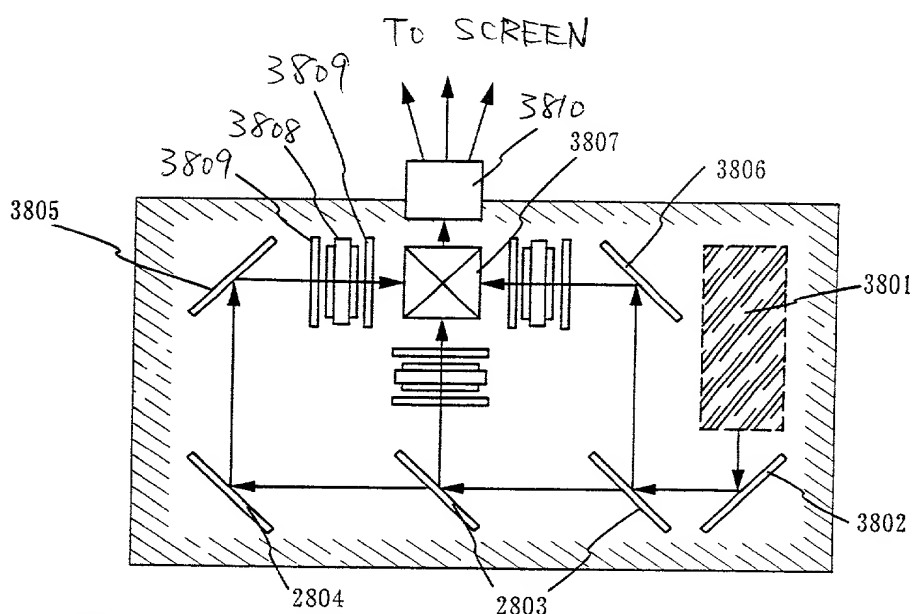
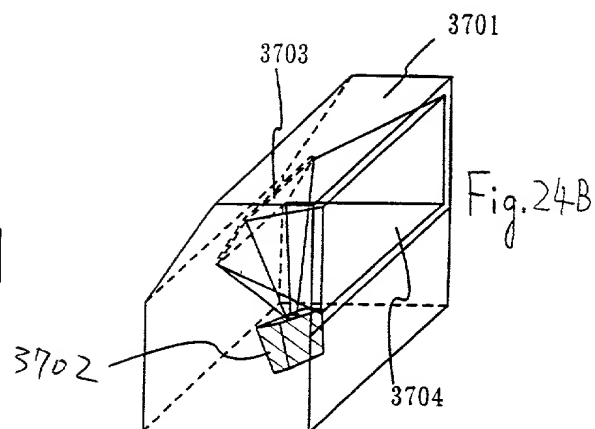
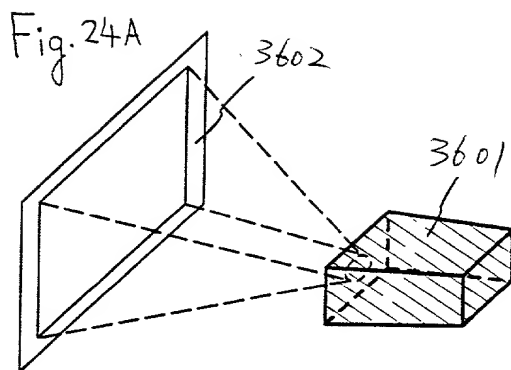


Fig. 24C PROJECTION DEVICE (THREE PLATE TYPE)

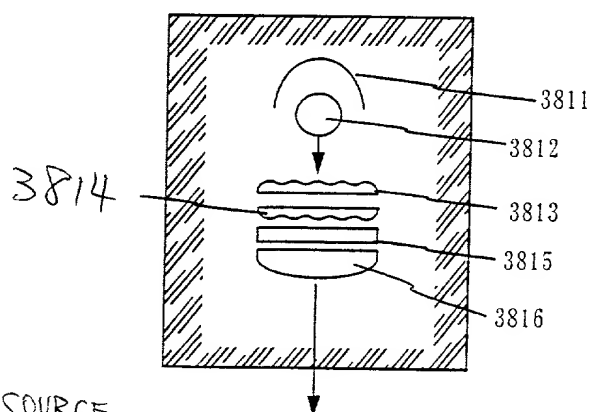


Fig. 24D LIGHT SOURCE OPTICAL SYSTEM

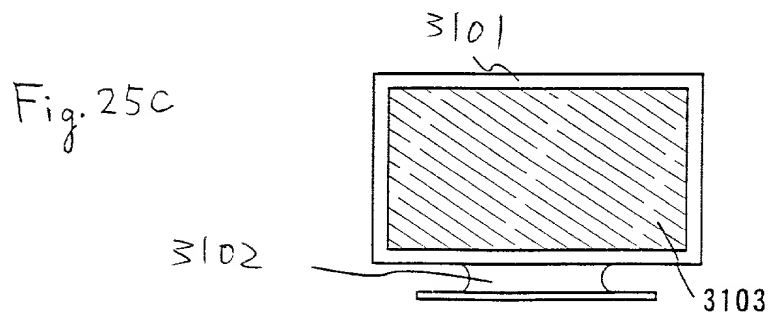
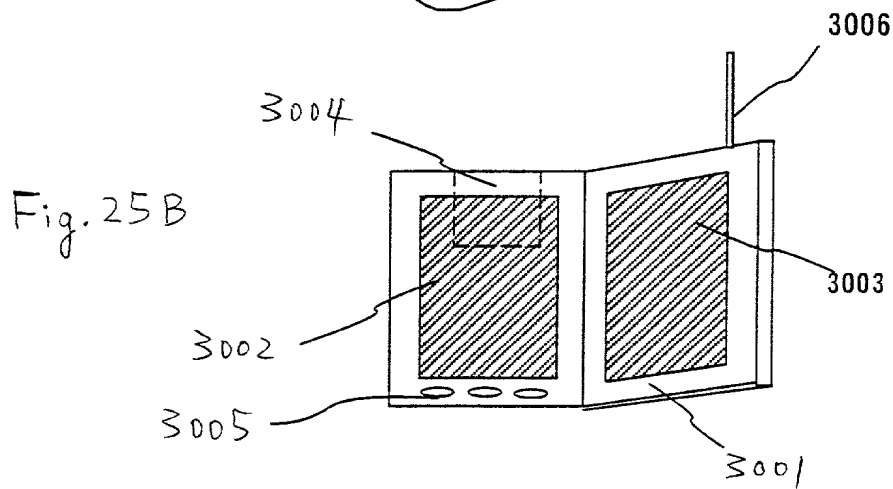
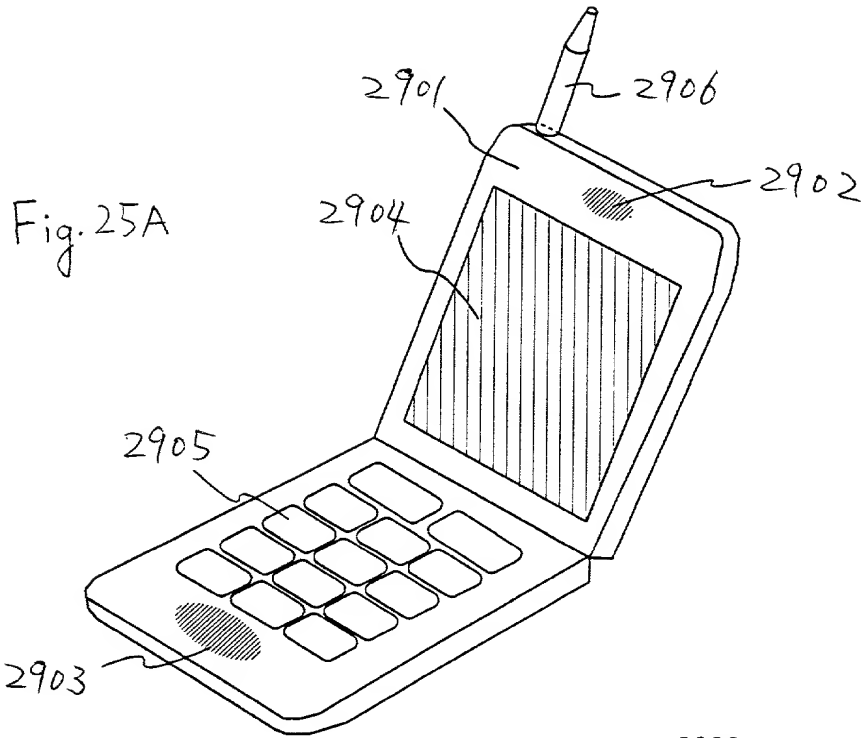


Fig. 26A

OVERLAPPED PORTION
OF LASER
IRRADIATION

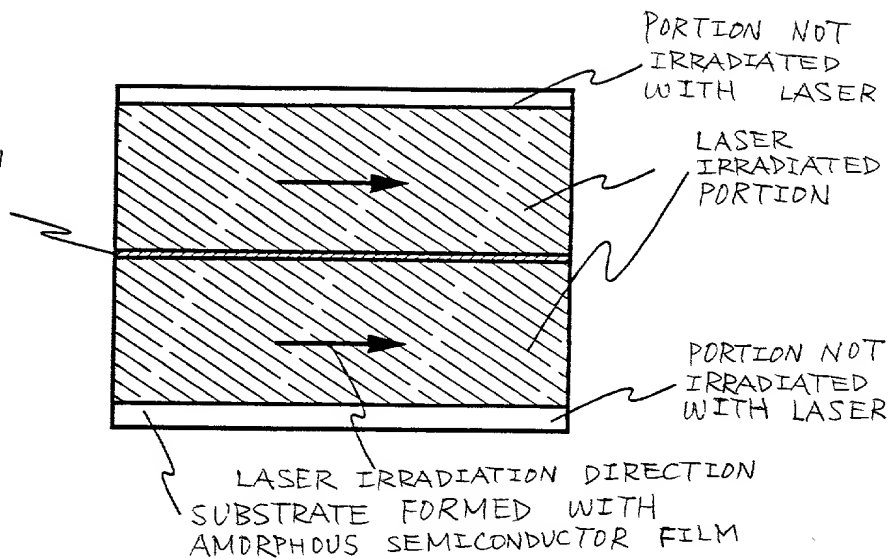


Fig. 26B

PORTION NOT
IRRADIATED
WITH LASER

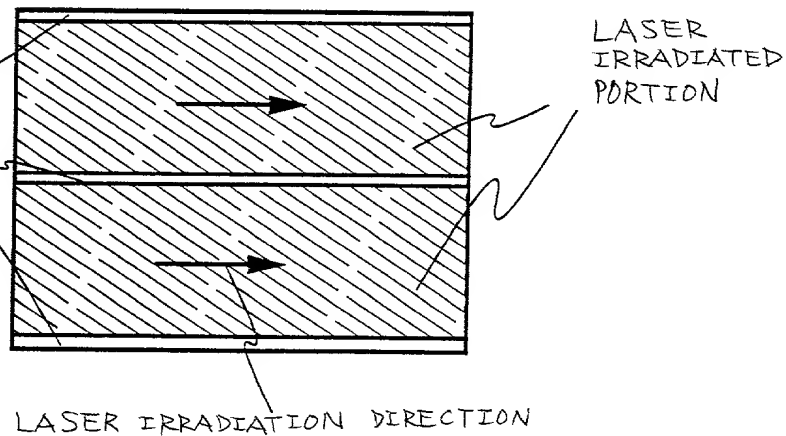


Fig. 26C

PORTION NOT
IRRADIATED
WITH LASER

